Lab 3

Finite State Machines

Reading

- Class notes on State Elements: Circuits That Remember

Exercises

Exercise 1

Consider the design of a finite state machine (FSM) with two 1-bit inputs (clk and CE), and one 2-bit output (X). clk is the clock signal and CE is the "count enable" signal. While CE=1, the FSM behaves as a "binary counter", i.e. its output cycles through the pattern 00, 01, 10 11, 00, moving from one output value to the next on each positive edge of clk. If CE = 0 the output value remains unchanged.

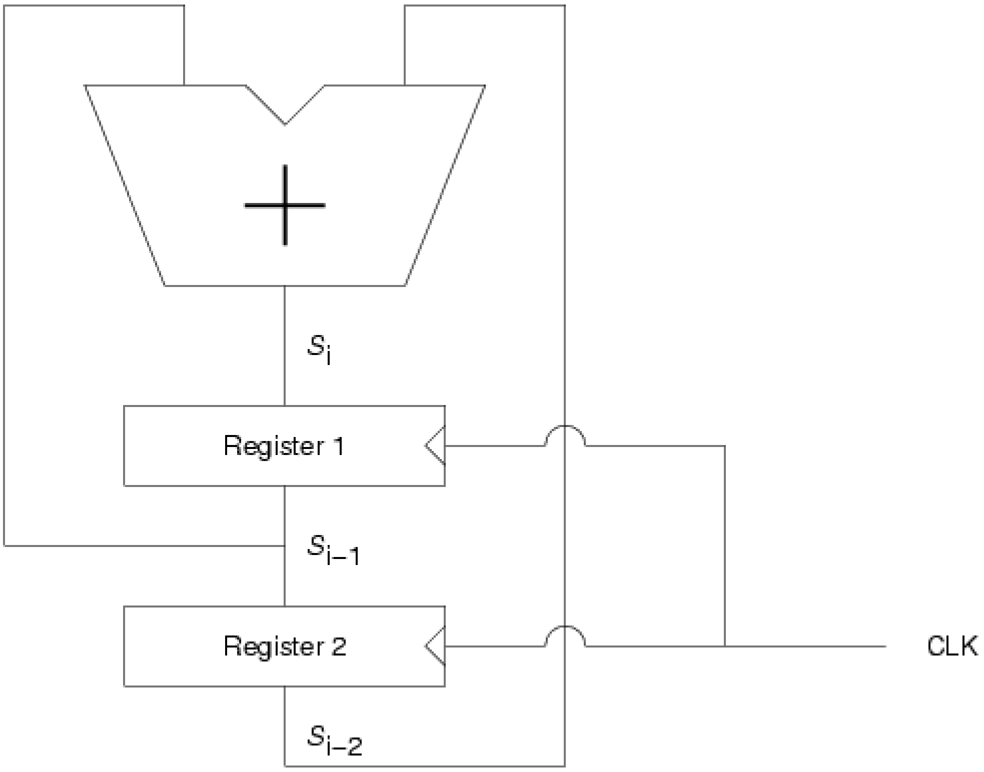
Note that FSM has no reset input signal. You can assume that it starts up in any legal state.

Sketch the state transition diagram that represents the behavior of this FSM in the style of the lecture notes.

Checkoff

Show your state transition diagram to your TA.	

Exercise 2



Draw the waveform diagram for the first 5 iterations of the above FSM (Refer to page 5 of the reading State Elements: Circuits That Remember). What operation does this FSM perform? Write a simple program in C which returns the value stored in "Register 2" as a function of the number of clock ticks since the FSM started. Display the first 10 values of "Register 2" in the first 10 cycles, one value per line.

Note: T_{add}, $T_{clk\text{-}to\text{-}q}$ and the clock period are exactly the same as on the example on page 5. I.e., T_{add} is double of $T_{clk\text{-}to\text{-}q}$, which are both much less than the clock period.

Initial State: Register 1 holds '1' and register 2 holds '0'.

Checkoff

Show waveform diagram of the FSM to your TA.	
Describe the operation of this FSM.	
Show and run your code that simulate "Register 2" to your TA	